JPE 18-2-11

https://doi.org/10.6113/JPE.2018.18.2.432
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Capacitor Voltage Boosting and Balancing using a TLBC for Three-Level NPC Inverter Fed RDC-less PMSM Drives

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Abstract

This paper presents a capacitor voltage balancing topology using a three-level boost converter (TLBC) for a neutral point clamped (NPC) three-level inverter fed surface permanent magnet synchronous motor drive (SPMSM). It enhanced the performance of the drive in terms of its voltage THD and torque pulsation. The main attracting feature of the proposed control is the boosting of the input voltage and at the same time the balancing of the capacitor voltages. This control also reduces the computational complexity. For the purpose of close loop vector control, a software based cost effective resolver to digital converter RDC-less estimation is implemented to calculate the speed and position. The proposed drive is simulated in the MATLAB/SIMULINK environment and an experimental investigation using dSPACE DS1104 validates the proposed drive system at different operating condition.

Key words: Capacitor voltage balancing, Multilevel inverter, Permanent magnet synchronous motor, RDC, Three-level boost converter, Vector control

I. INTRODUCTION

Vector controlled PMSM drives brought renaissance to variable speed drives, replacing traditional scalar-controlled drives. In industrial drives, two-level inverters are generally used to feed PMSMs. However, in the case of two-level inverters, the switching frequency is one of the main concerns in regards to the size of the passive components, the superior control of the electric drives and the proliferation power density of the inverter [1]-[5]. On contradictory, higher switching frequencies may lead to higher switching losses in two-level inverters, which results in inferior inverter efficiency. When compared to two-level inverters, three-level inverters produce lower switching losses at higher switching frequencies to get the same dc-link voltage [4], [6]-[9]. Another attractive feature is the reduction in the total harmonic distortion. A lower dv/dt also reduces the voltage stress across the power switches. A significant reduction in the torque ripple is achieved with use of a three-level inverter [10]. Satisfying the application demand, PMSM bring the keen attention of the Electric vehicle manufacturer as it is one of the most preferred choices for electric and plug-in hybrid EV applications. This is due to its fast torque response and high torque to weight ratio when compared with induction motors. To drive a machine a three-level inverter has become the preferred choice for replacing conventional two-level VSIs. The combination of a three-level inverter and a PMSM allow it to operate with an increasing dc bus voltage. However, voltage unbalancing across the capacitor is the main drawback of the NPC inverter [11]. Researchers have exerted extensive effort to overcome this problem and they have developed several voltage balancing technique. A self-balancing technique for three-level inverters is presented in [12].

However, a self-balancing technique is not always adequate since slight variations in the system parameters causes drifts in the neutral-point voltage. Carrier PWM and space vector modulation based voltage balancing techniques are studied in [13]-[24]. However, modified PWM techniques increase the computational complexity. A balancing circuit is added to a NPC inverter for simple computational control. A number of

Manuscript received Apr. 5, 2017; accepted Oct. 21, 2017
Recommended for publication by Associate Editor Jaehong Kim.
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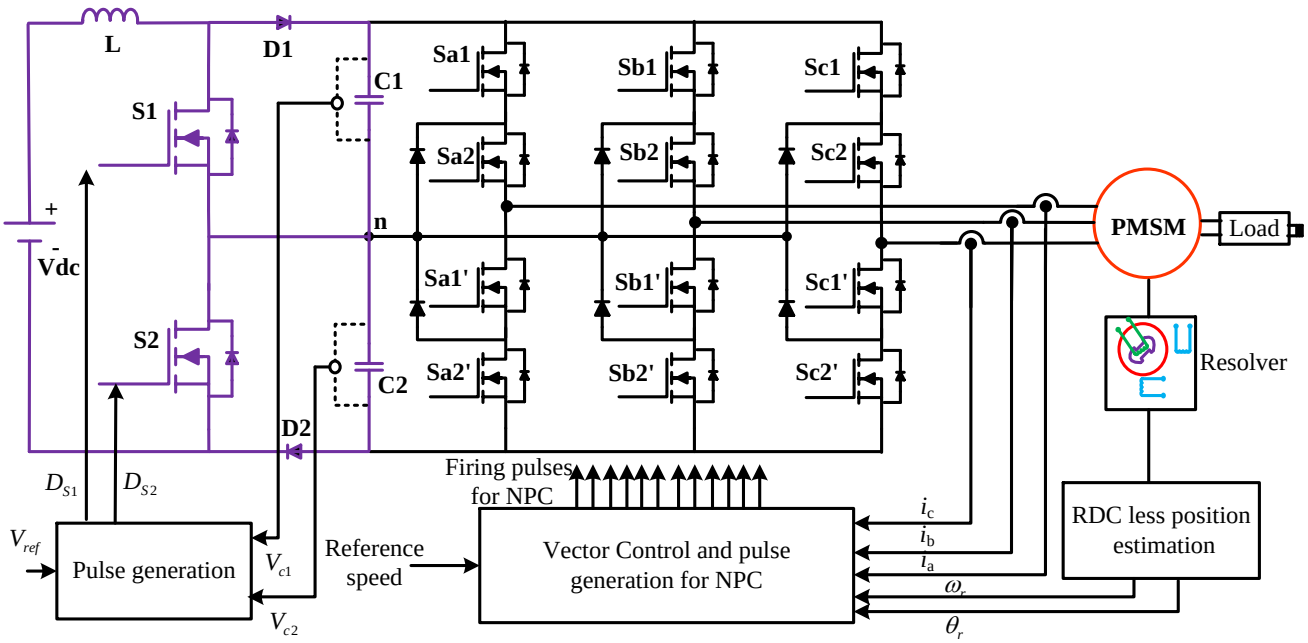


Fig. 1. Schematic diagram of the proposed PMSM drive system.

detailed studies based on the balancing circuit are presented in [25]-[30]. A DC-link capacitance minimization technique is discussed in [31].

An unbalance of the dc link occurs in NPC fed PMSM drives operating in different modes of operation with changes in the speed or torque by the demands of an application. To maintain dc balancing, the three-level boost converter (TLBC) is the most attractive circuit used in conjunction with the three-level NPC inverter. The advantageous features include a reduction in the switching losses and lower reverse recovery losses of the diode when compared with conventional boost converters (CBC). The use of a TLBC with a three level NPC can effectively reduce the computational complexity more than implementing carrier PWM and space vector modulation based voltage balancing techniques. The wide range of electric vehicles, water pumping systems and propulsion systems is powered by batteries or photovoltaic cells, which requires a dc-dc converter for stepping up the voltage levels for the drives [32]. This paper presents the addition of a TLBC circuit with a three level NPC fed PMSM, which can maintain the dc balancing and provide boosting of the input voltage level.

Based on previously presented literature reviews, most of the studies on three-level NPC inverted fed PMSM motor drives mainly focus on the investigation of capacitor voltage balancing while boosting of the input voltage. PM motors with a fast dynamic response, good speed regulation and high efficiency demand information of the rotor position to implement the vector control [33]-[35]. The rotor position can be accurately measured by using a resolver sensor. Since 1991 several researchers have presented ideas on the manifolds of proposed drives with a resolver sensor [36]-[39]. However, all of these articles are mainly focused on improvements of the measurement accuracy of the RDC. Therefore, implementation with complete drive system without a RDC is still a fascinating area for researchers.

The proposed drive system consists of four major components: a NPC inverter with a TLBC circuit, a PMSM, position estimation and control for the drive system. The complete drive system has been shown in Fig. 1. The TLBC circuit has been used to balance the capacitor voltage of the NPC inverter which is described in section II. In addition, the firing pulses for the NPC inverter are generated by implementing the vector control. Section III gives a detailed description of the RDC-less position estimation, which provides the necessary information in terms of the position (θ_r) and speed (ω_r) estimation to implement the vector control. A description of the vector control is not presented in this paper since it was considered in [40]. Simulation and experimental studies are carried out for the proposed PMSM drive system under different operating conditions. A laboratory prototype has been fabricated to implement the experimental system. dSPACE DS1104 is used to generate all of the control pulses for the proposed drive system.

II. Operation of TLBC

DC-link capacitor (C_1 and C_2) voltage balancing is achieved using a three-level boost converter. Due to some attractive feature such as reduced switching losses and reduced recovery voltage of the diode, the TLBC has drawn

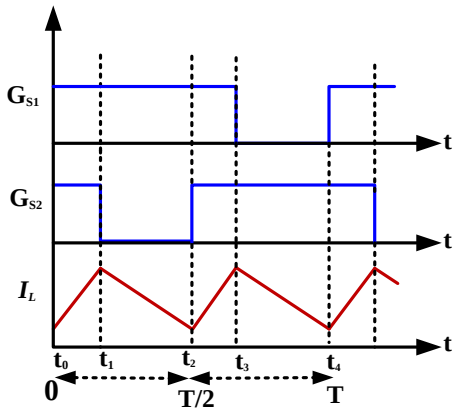


Fig. 2. Firing signals of the two switches and inductor current of the TLBC.

the keen attention of researchers and technologist for high power applications. The inductor current ripple is also less. This requires a smaller size inductor when compared to the conventional boost converter. One inductor L and two switches S_1 & S_2 with two diodes D_1 and D_2 are used as the balancing circuit for the three-level NPC inverter.

The output voltage equation of the TLBC is given as [25]:

$$V_0 = V_{c2} + V_{c1} = \frac{2V_{dc}}{(2-D)} \tag{1}$$

D represents the duty ratio. It is varied from 0 to 1.

The equation of the current ripple in case of the conventional boost converter is:

$$\Delta I = \frac{V_{dc} D T_{SW}}{L} \tag{2}$$

T_{SW} represents the switching period.

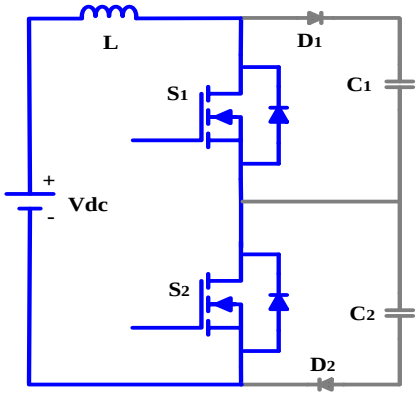
The current ripple of the three-level boost converter is:

$$\Delta I = \frac{V_0(1-V_{dc}/V_0)(2V_{dc}/V_0 - 1)}{2Lf_{SW}} \tag{3}$$

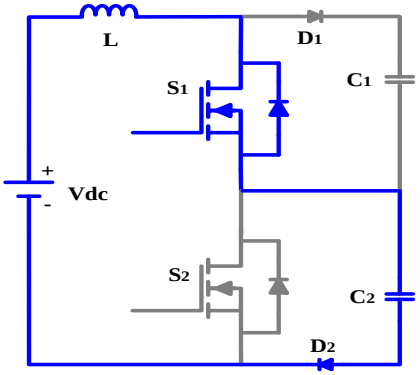
Comparing the above equations it is observed that the current ripple in the TLBC is 50% less than that of the conventional one.

A typical firing signal of the two switches is shown in Fig. 2. A circuit diagram of the TLBC at different operating modes is shown in Fig. 3. It is observed that both S_1 and S_2 are ON during the periods $t_0 < t < t_1$ and $t_2 < t < t_3$. The inductor current flows as marked by the blue line shown in Fig. 3(a). At this time energy is stored in the inductor.

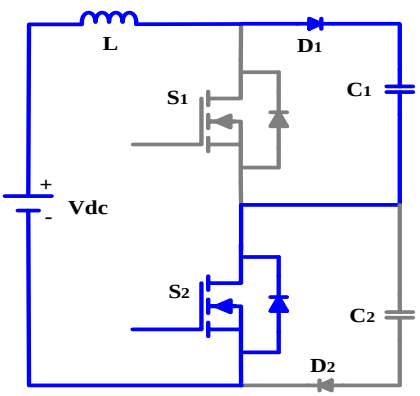
The switch S_1 is ON and the switch S_2 is OFF during the period $t_1 < t < t_2$. In this time period, the capacitor C_2 is charged. Therefore, the voltage across the capacitor V_{C2} increases. The inductor stored energy is transferred to C_2, and the inductor current is gradually reduced. At the time period $t_3 < t < t_4$ the switch S_1 is OFF and the switch S_2 is ON. At this time, the capacitor C_1 gets charged and V_{C1} is increases. The inductor current is gradually reduced at this time.



(a) $t_0 < t < t_1$ and $t_2 < t < t_3$.



(b) $t_1 < t < t_2$.



(c) $t_3 < t < t_4$.

Fig. 3. Capacitor voltage balancing using the TLBC for the entire time period T.

A schematic diagram of the dc capacitor voltage balancing and boosting is shown in Fig. 4. The proper value of D must be selected to maintain the boosting of the input dc at the desired voltage level by using (1). This can alternatively charge the capacitors C_1 and C_2 and make them theoretically balanced. In practical applications, the parameters of the components are not exactly balanced due to the various modes of operation and transient conditions of NPC fed

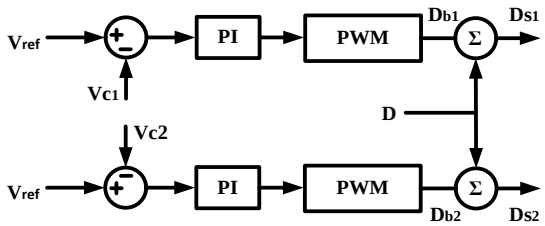


Fig. 4. Schematic diagram of the capacitor voltage balancing circuit of the TLBC circuit.

PMSM drives. To ensure equal voltages on C_1 and C_2, a voltage balancing circuit is used as shown in Fig. 4. The individual balancing control has been implemented for both of the capacitors. The voltages V_{c1} and V_{c2} are separately compared with the magnitude of reference voltage V_{ref} and the errors are processed through a proportional integral (PI) controller. The output of the PI controller is processed through PWM to evaluate the duty ratios for balancing the capacitor voltages. The duty ratios D_{b1} and D_{b2} have been added to D, which is selected for the desired output voltage of the dc link, to determine the duty ratios for the switches S_1 and S_2, respectively.

III. RDC-LESS POSITION SENSING FOR THE PROPOSED DRIVE

The working principle of the resolver is quite similar to that of the transformer. Construction wise, the resolver has three windings. The primary winding of the resolver is a rotating coil. The two secondary coils are stationary and are placed in the stator 90˚ apart from each other. This position sensor can measure the initial accurate rotor position at standstill. In general, a resolver to digital converter (RDC) is required to estimate the rotor position. However, software based position estimation is achieved for the proposed drive system without using a RDC. A high-frequency signal is applied to excite the primary coil of the resolver. With the rotation of the rotor, the induced emf in the secondary coils helps measure the actual position. Finally, the rotor position estimation is done by demodulating the output signal of the resolver. The schematic of RDC-less position estimation is shown in Fig. 5.

The frequency of the two output sine and cosine signal is the same as the frequency of the excitation signal. However, the amplitude variation depends on the shaft angle. Instead of using a RDC, the resolver algorithm proposed for the drive system is software based. The equations related to the primary and secondary winding are defined as:

$$V_{in}(t) = \hat{V}_{in}.\sin\omega_{ref}t \tag{4}$$

$$V_{o1}(\phi,t) = \hat{V}_{in}.k.\sin\phi.\sin\omega_{ref}t \tag{5}$$

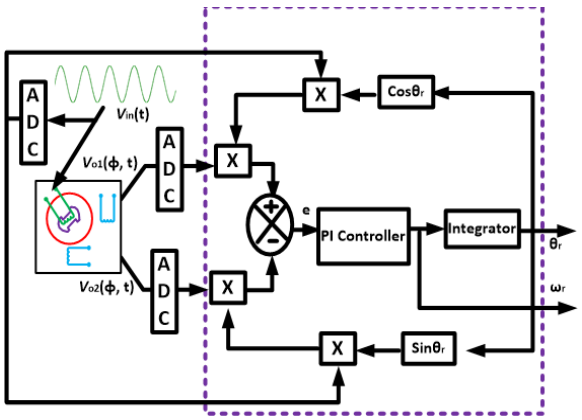


Fig. 5. Schematic of the RDC-less position estimation.

$$V_{o2}(\phi,t) = \hat{V}_{in}.k.\cos\phi.\sin\omega_{ref}t \tag{6}$$

Where, k is the turn ratio of the resolver, $\hat{V}_{in}$ implies the peak value, ϕ is the rotor position in rad, and ω_{ref} is the frequency of the excitation signal in (rad/sec).

The error signal nearest to zero is the difference between the actual angle (Φ) and the computed angle (θ). The feedback loop and PI controller provide the speed ω_r. The rotor position θ_r is obtained by the integration of the motor speed.

The error calculation is based on the following trigonometric relation given by:

$$\left.\begin{aligned} e = (\hat{V}_{in}.\sin\omega_{ref}t.\cos\theta)(\hat{V}_{in}.k.\sin\phi.\sin\omega_{ref}t) - \\ (\hat{V}_{in}.\sin\omega_{ref}t.\sin\theta)(\hat{V}_{in}.k.\cos\phi.\sin\omega_{ref}t) \end{aligned}\right\} \tag{7}$$

$$e = V_{in}(t).(\hat{V}_{in}k.\sin\omega_{ref}t)\{\sin\phi\cos\theta - cos\phi\sin\theta\} \tag{8}$$

$$e = A.\sin(\phi-\theta) \tag{9}$$

$$A = V_{in}(t).(\hat{V}_{in}k.\sin\omega_{ref}t) \tag{10}$$

IV. SIMULATION AND EXPERIMENTAL RESULTS

The specifications of the proposed PMSM drive in this study are listed in Table I. The proposed PMSM drive with a resolver sensor is simulated and experimentally validated using a three level boost converter (TLBC) with a neutral point clamped (NPC) three-level inverter.

A. Simulation Results

Initially the drive has been simulated with a three-level NPC inverter without the TLBC circuit with an input dc voltage of 300 V. It is noticed that when the drive is operated without the voltage balancing circuit, the capacitor voltages across the two capacitors are unequal.

However the potential difference between the two capacitors C_1 and C_2 is small at the no load condition. This difference increases at transient operation of the drive. It is

TABLE I
PARAMETERS OF THE DRIVE SYSTEM

Input dc voltage (V_{dc})	200 V
Inductance of TLBC (L)	7 mH
Capacitance of C_1 and C_2	2200 μF
Voltage across capacitor C_1 and C_2	150 V
Stator phase resistance (R_S)	2.55 Ω
Torque Constant	0.75 Nm/A
Phase inductance (L_d, L_q)	5.15 mH
Moment of inertia (J)	0.000062 kg-m^2
Total load inertia	0.001914 kg-m^2
No of poles (p)	8
Damping friction	0.0041N-m/rad

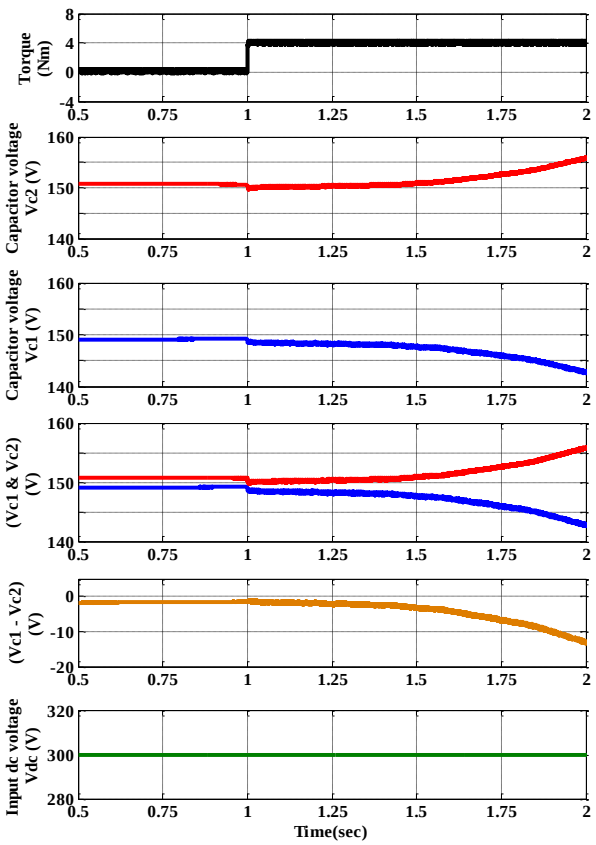


Fig. 6. Simulation results of capacitor voltages at the loading condition without the TLBC circuit.

observed that when a load of 4 Nm is applied at time t = 1s, the difference between the two capacitor voltages V_{C1} and V_{C2} is gradually increased. Trace 1 in Fig. 6 shows the torque, whereas trace 2 and trace 3 represents the capacitor voltages V_{C1} and V_{C2} across the two capacitors C_1 and C_2. The deviations of the voltages of the two capacitors are shown in trace 4. The potential difference between the two capacitors is shown in trace 5. It is observed that the potential difference gradually increases after the loading instant.

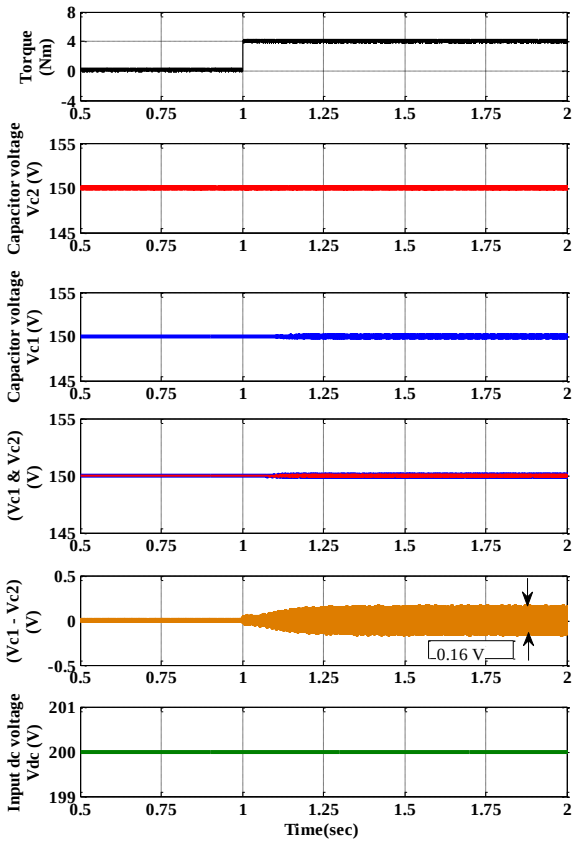


Fig. 7. Simulation results of capacitor voltages at the loading condition with the TLBC circuit.

To overcome the capacitor voltage balancing problem, a three-level boost converter (TLBC) circuit has been implemented. Capacitor voltages with the load changing operation are shown in the Fig. 7. It is observed that during the no-load operation both of the capacitor voltages are maintained to the reference value 150 V. It is also noticed that during the loading operation both of the capacitor voltages are equally maintained at 150 V with a fluctuation limit of ±0.18 V. The input voltage to the NPC inverter is maintained at 300 V, which is the sum of the two capacitor voltages with the help of the TLBC by selecting a duty ratio (D) of 0.667. The input dc voltage (V_{dc}) for the TLBC circuit is selected as 200 V. Therefore, the proposed three-level NPC inverter fed PMSM drive with the TLBC circuit provides an added advantageous boosting feature in addition to the capacitor voltage balancing.

The voltages V_{C1} and V_{C2} across the two capacitors C_1 and C_2 are depicted by trace 2 and trace 3 in Fig. 7. It is noticed that the equal voltage sharing is done by both of the capacitors. Both of the voltages V_{C1} and V_{C2} are presented in trace 4 to show the difference between the two capacitor voltages. However, the potential difference between the two capacitors is very less which is shown in trace 5.

The performance of the proposed drive is investigated at different operating conditions. Fig. 8 shows the starting

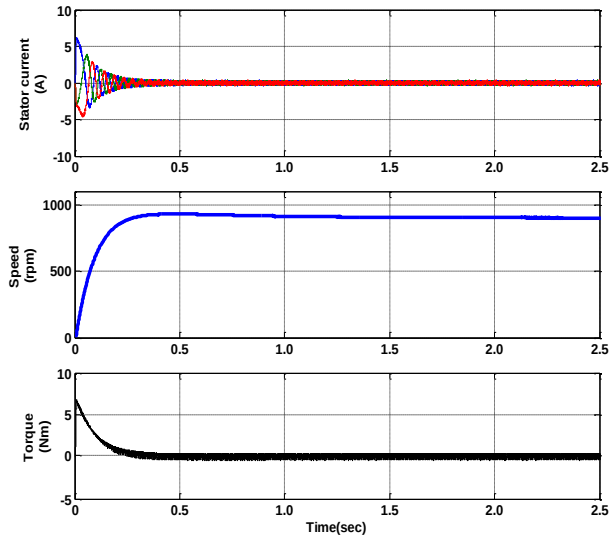


Fig. 8. Simulation result of the starting response of a PMSM drive.

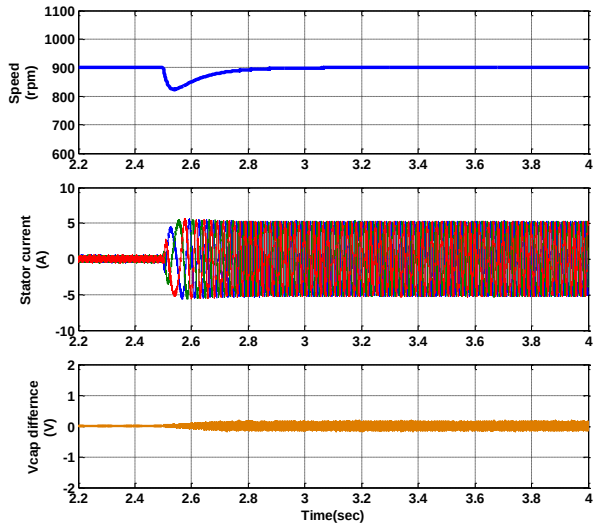


Fig. 9. Simulation result of a PMSM drive at load changing.

response of the drive. The reference value of the speed is kept at 900 rpm and the motor is started with no load. Initially the starting current is high. However, it is reduced as the motor reaches its reference speed value. Simulation results with the load changing in the proposed drive are shown in Fig. 9. It is observed that when a 4 Nm load is applied the current is increased. At this instant, the speed is slightly reduced. However, it reaches its reference value by the closed loop operation of the drive. It is also observed that the proposed drive maintained capacitor voltage balancing in case of the load changing operation. The performance of the proposed drive with vector control at the speed changing operation has also been investigated.

The speed reference increased from 900 rpm to 1200 rpm. A change in the speed reference of 300 rpm has been applied. The response of the drive at the speed changing operation has

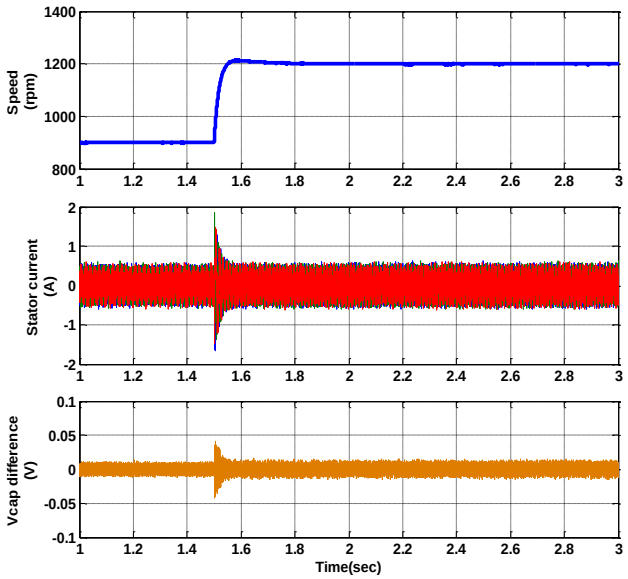


Fig. 10. Simulation result of a PMSM drive at speed changing.

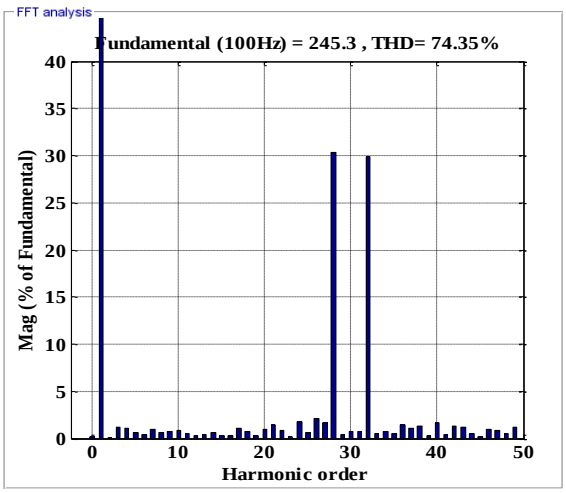


Fig. 11. Voltage THD of a two-level inverter fed PMSM.

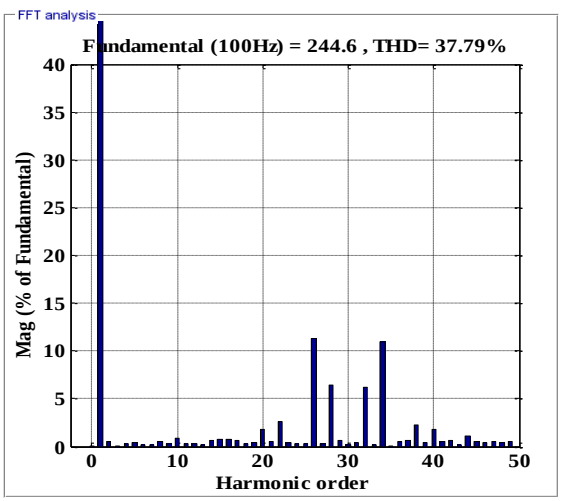


Fig. 12. Voltage THD of a three-level NPC inverter fed PMSM.

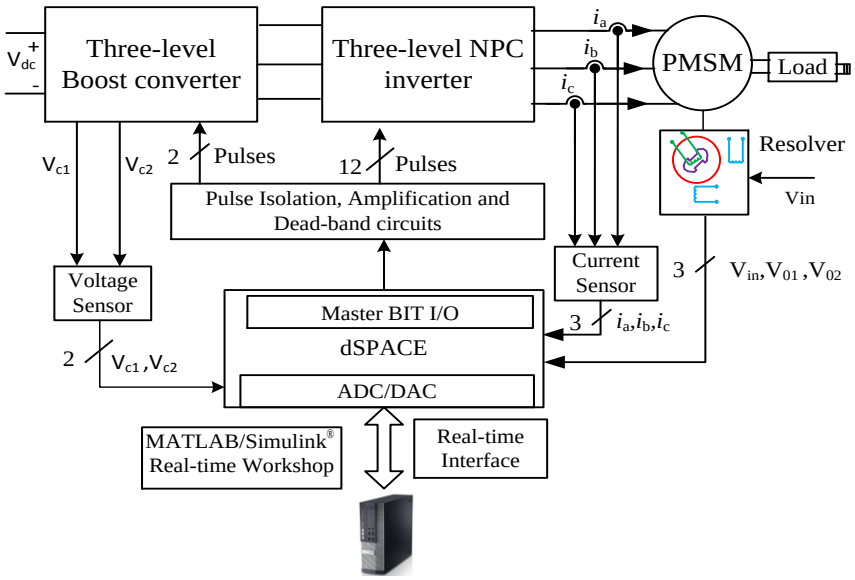


Fig. 13. Schematic diagram of a hardware implementation of the proposed drive system.

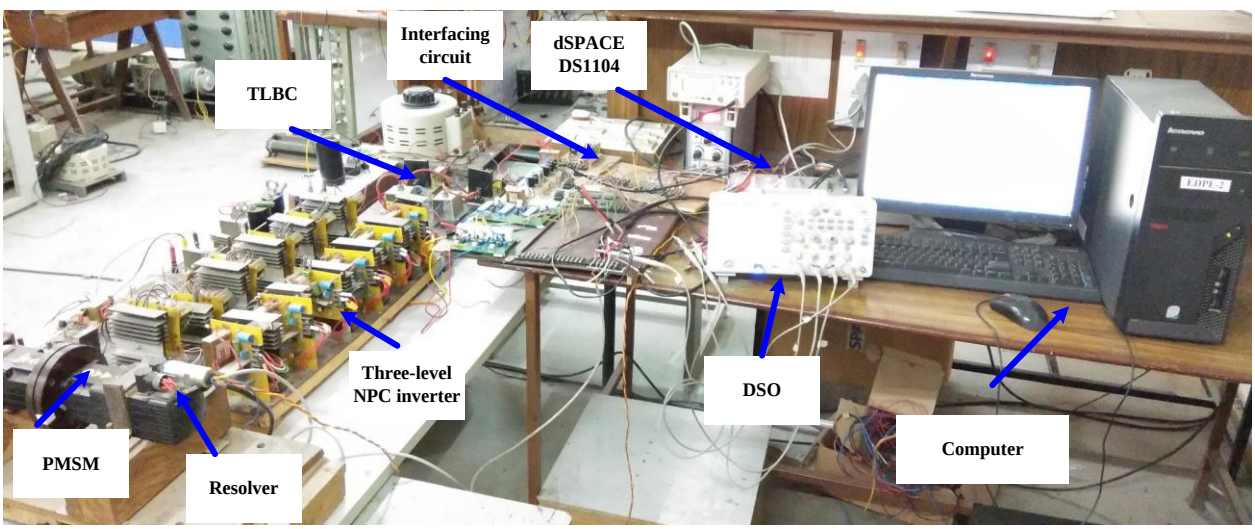


Fig. 14. Experimental setup.

been shown in Fig. 10. At t = 1.5s, the speed reference has been increased from 900 rpm to 1200 rpm. At this time, the torque is increased by the motor to reach the reference speed. As a result, the stator current is also slightly increased at that time. The torque is reduced once the reference speed value is reached. The capacitor voltage difference at the time of the speed increasing operation is shown in Fig. 10. The simulated results clearly show that the potential difference between the two dc-link capacitors are very less i.e. below 0.1 V. When the PMSM motor is fed with a three-level inverter, the voltage THD is improved when compared to the two-level inverter. In case of a PMSM motor with a two-level inverter the voltage THD is 74.35%, which is shown in Fig. 11. However, with the three-level inverter, the voltage THD is 37.79% as shown in Fig. 12. It is observed that three-level inverter provides nearly a 50% lower total harmonic distortion when compared to the conventional two-level inverter.

B. Experimental Verification

In order to verify the simulation of the proposed three-level NPC inverter fed PMSM drive, the following prototypes have been developed in the laboratory. a) Three-level neutral point clamped inverter power circuit. b) Capacitor voltage balancing circuit with a three-level boost converter. c) The control circuit consisting of a dead-band circuit, dc power supplies, voltage, and current sensor circuits. A schematic diagram for the hardware implementation of the three-level NPC inverter fed PMSM drive system is shown in Fig. 13. As a first step towards the hardware development, a three-level NPC inverter

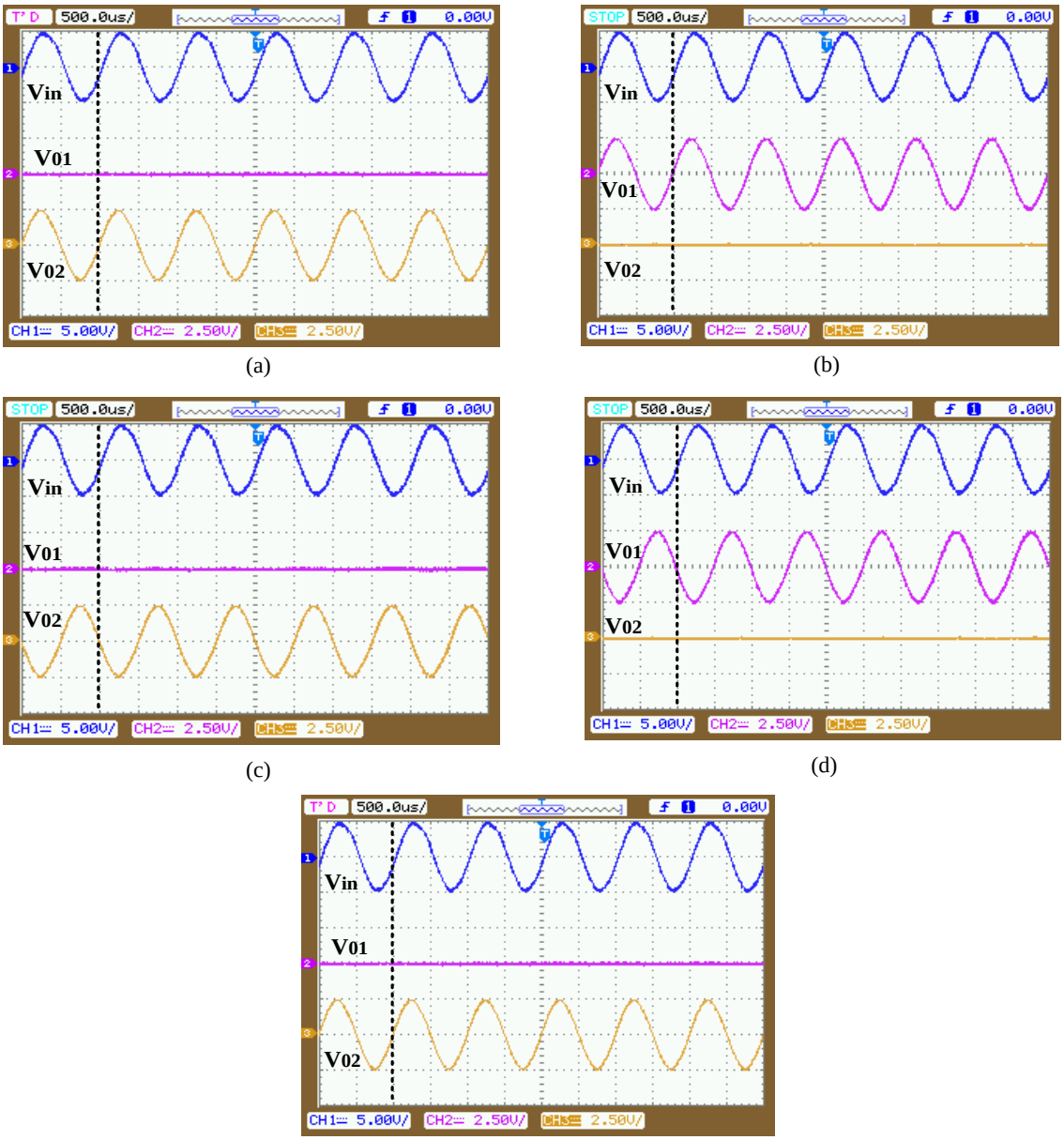


Fig. 15. Experimental results of the resolver output signal at: (a) 0^o shaft rotation, (b) 90^o shaft rotation, (c) 180^o shaft rotation, (d) 270^o shaft rotation, (e) 360^o shaft rotation.

has been designed and constructed to feed a surface permanent magnet synchronous motor. A voltage balancing circuit using a three-level boost converter is also designed and constructed. A gate driver circuit for the power electronic switches was also designed. For the development of the power circuit, MOSFETs (IRFP460) have been used as switching devices. The experimental setup is shown in Fig. 14. Vector control has been implemented to generate the firing pulses to the three-level NPC inverter. A dSPACE DS1104 controller has been used in the proposed drive system. A software based position estimation algorithm provides the necessary position and speed information.

Accurate position information plays a key role in implementing the vector control of a PMSM drive. The rotor position of the PMSM can be measured by using a resolver without a RDC to make a cost effective drive. The output signal of the resolver at complete 360˚ rotation of the rotor shaft is shown in Fig. 15. From the experimental results shown in Fig. 15(a), it is observed that the sine output signal is zero and that the cosine signal is in phase with the input signal at the starting position when the angle is zero. Channel 1 represents the input high frequency excitation signal of the resolver. Channels 2 and 3 represents the sine and cosine outputs of the resolver. The variation in the output signal by a 90˚ rotation of the rotor shaft is shown in the Fig. 15(b). At this position, the sine output signal is in phase with the input

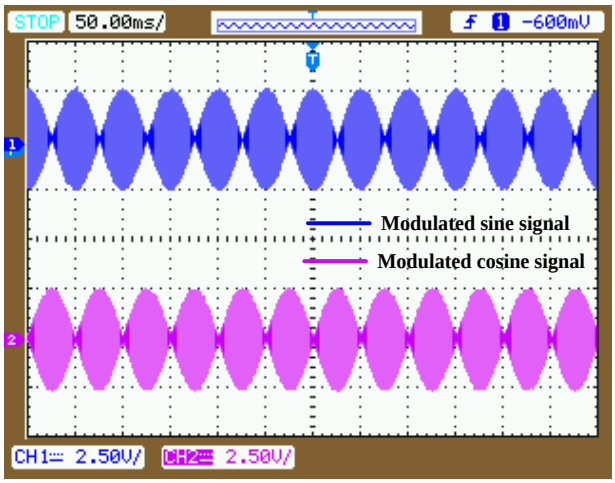


Fig. 16. Experimental results of a modulated sine and cosine output signal.

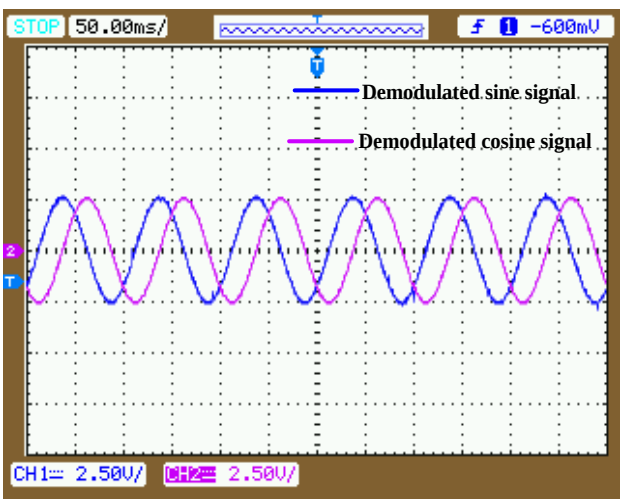


Fig. 17. Experimental results of a demodulated sine and cosine signal.

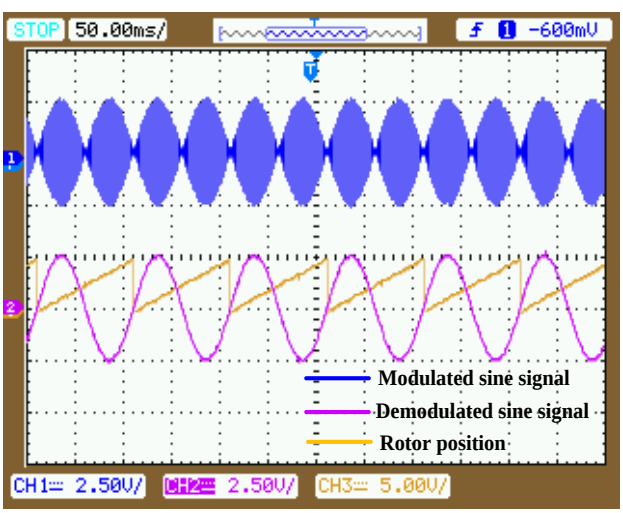


Fig. 18. Experimental results of demodulated and modulated sine waves with the position angle of the rotor shaft.

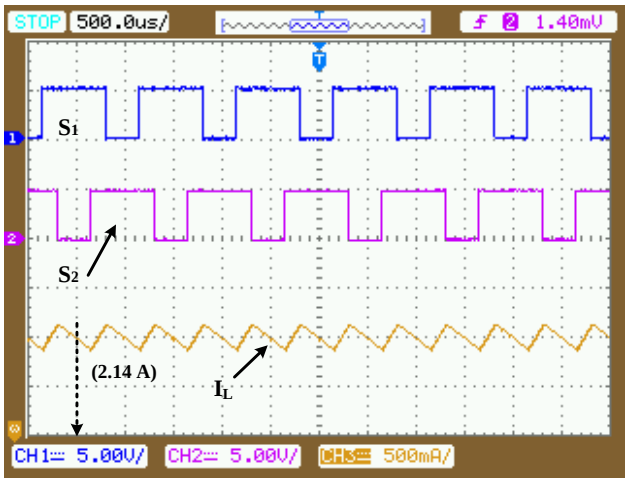


Fig. 19. Experimental waveforms of the inductor current and switching pulses for a three-level boost converter (pulses to S_1 and S_2 5V/div and inductor current 500mA/div).

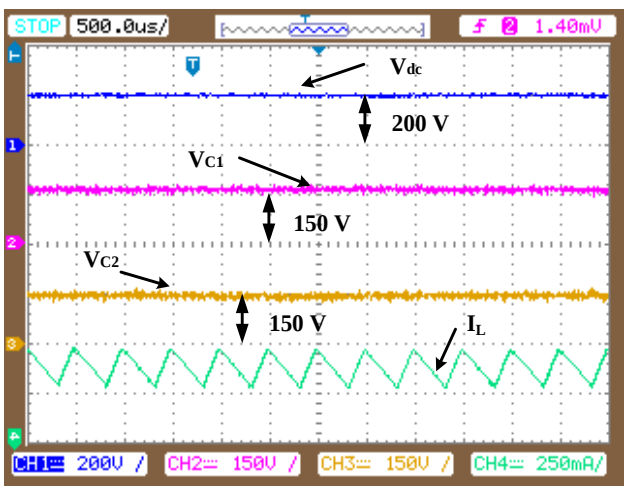


Fig. 20. Experimental waveforms of the input voltage, output capacitor voltages and inductor current of a three-level boost converter (capacitor voltage 150V/div, input dc voltage V_{dc} 200V/div, inductor current 250mA/div).

signal and the cosine signal is zero. From Fig. 15(c) it can be observed that the sine output signal is zero and that the cosine signal is in the opposite phase when the input signal is at a 180° rotation of the rotor shaft. The cosine output signal is zero and the sine signal is in the opposite phase when the input signal is at a 270° rotation of the rotor shaft as shown in Fig. 15(d). Furthermore, from Fig. 15(e) it can be observed that the sine output signal is zero and the cosine signal is in phase when the input signal is at 360°.

To excite the primary coil of the resolver, a high frequency signal is applied. With the rotation of rotor, the resolver induces two modulated signals. These modulated signals are demodulated using the estimation algorithm discussed in section III. Trace 1 in Fig. 16 denotes the modulated output sine signal, and trace 2 denotes the modulated output cosine signal. Fig. 17 shows the demodulated sine and cosine output

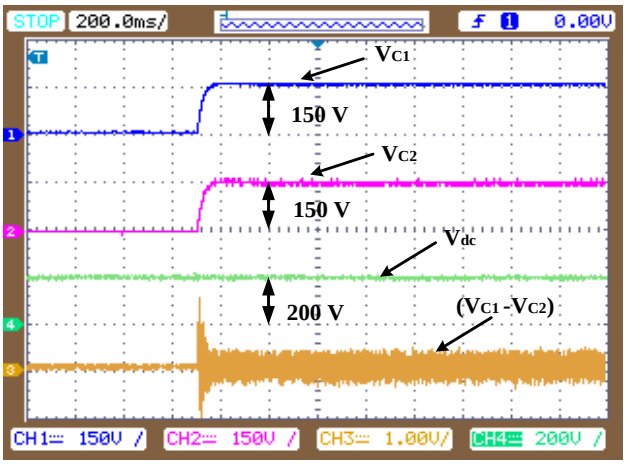


Fig. 21. Experimental result of the capacitor voltage boosting and balancing (capacitor voltage 150V/div, input dc voltage 200V/div, capacitor voltage difference 1V/div).

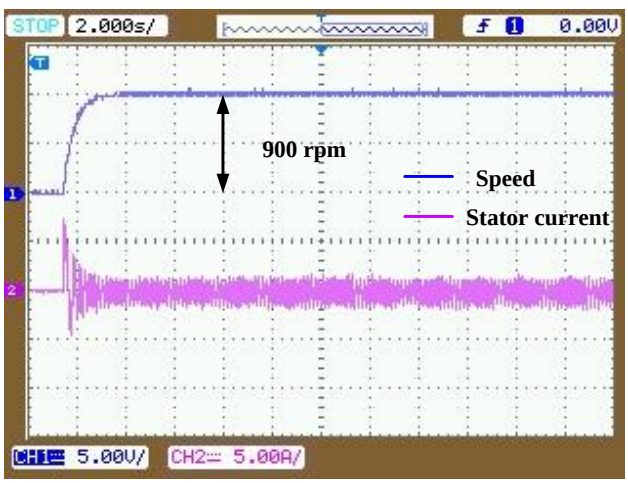


Fig. 22. Experimental result of the starting response of a PMSM drive (speed 450 rpm/div and stator current 5A/div).

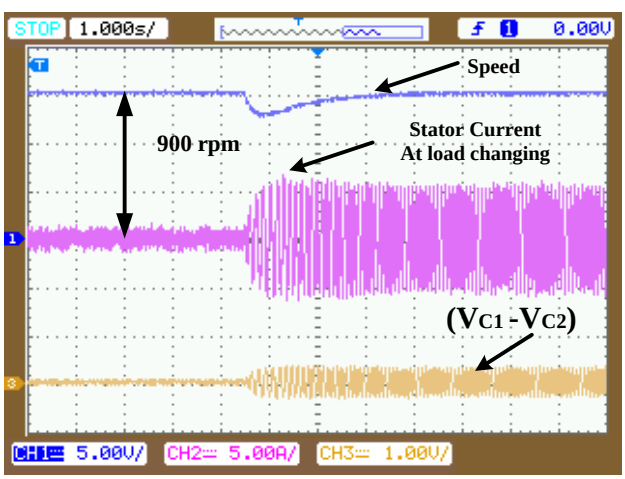


Fig. 23. Experimental result of a PMSM drive at load changing (speed 300rpm/div, stator current 5A/div, capacitor voltage difference 1V/div).

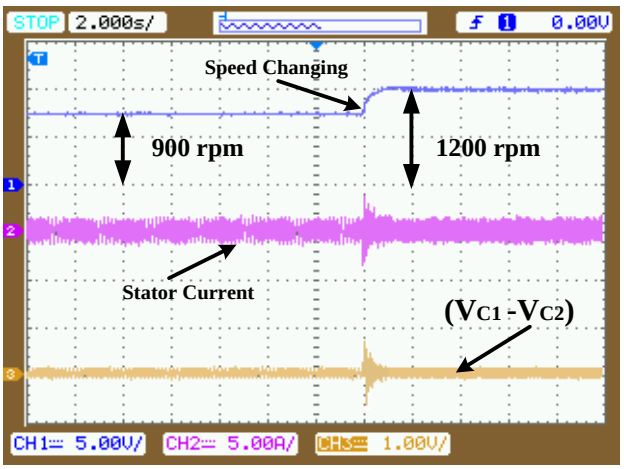


Fig. 24. Experimental result of a PMSM drive at speed changing (speed 600rpm/div, stator current 5A/div, capacitor voltage difference 1V/div).

signals. Experimental results of the rotor position with respect to the demodulated sine signal are shown in Fig. 18. The demodulated sine and cosine output provides θ_r with the help of the resolver algorithm discussed in section III. The actual rotor position θ_r and speed ω_r are used to run the PMSM motor with vector control. Whereas the firing pulses for the TLBC converter can be generated by the control circuit shown in Fig. 4.

The firing pulses generated for the switches (S_1 and S_2) of the TLBC are shown in Fig. 19, with a duty ratio (D) of 0.667 at the steady state condition of the load applied on the PMSM drive. The average value of the input inductor current (I_L) is 2.14 A, with upper and lower limits of ± 0.12A at the loading condition of 4 Nm as shown in Fig. 19. Fig. 20 depicts the input voltage (V_{dc}), and the voltage across capacitors C_1 and C_2. Their values are 200V, 150V and 150V, respectively. Experimental results of the capacitor voltage balancing are shown in Fig. 21. Channel 1 represents the voltage across the capacitor C_1 (with a scale of 150V/div) and channel 2 represents the voltage across capacitor C_2 (with a scale of 150V/div). It is observed that with the use of the TLBC in a three-level NPC inverter, the voltages across the capacitors are maintained at the desired value of 150 V.

The voltage difference shown in channel 3 (with a scale of 1V/div) is significantly less. Therefore, the dc link voltage is perfectly balanced with the use of the TLBC in a three-level NPC inverter. The input dc voltage (V_{dc}) is shown in channel 4 (with a scale of 200V/div).

The starting response of the proposed drive system is shown in Fig. 22. Trace 1 shows the speed response of the PMSM (with a scale of 450 rpm/div) and trace 2 represents the stator current (with a scale of 5A/div). The performance of the drive with load changing (4 Nm) is shown in Fig. 23. It is observed that the stator current is increased at the time of

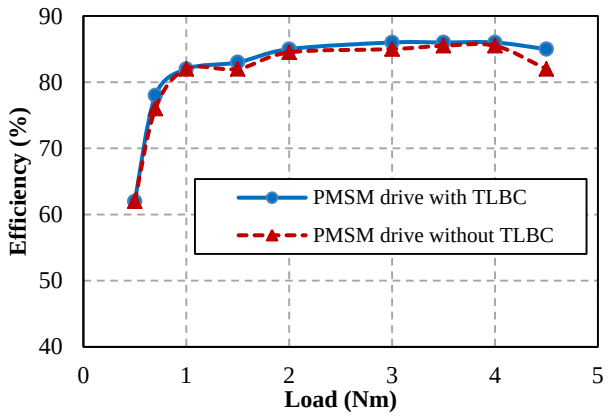


Fig. 25. Efficiency of the proposed PMSM drive.

loading which is presented in channel 2 (with a scale of 5A/div). It is also observed that there is dip in the speed response. This dip is due to the loading. This speed response, presented in channel 1 (with a scale of 300 rpm/div), reaches the reference due to the closed loop operation of the drive. Experimental results of the voltage difference between the two capacitors are presented in channel 3 (with a scale of 1V/div). It is also noticed that the proposed drive maintains the capacitor voltage difference within the desired value. Experimental results of the drive at the speed increasing operation are shown in Fig. 24. The speed of the motor is presented in channel 1 (with a scale of 600 rpm/div). The speed reference has been increased from 900 rpm to 1200 rpm. The stator current is presented in channel 2 (with a scale of 5A/div). The capacitor voltage difference is presented in channel 3 (with a scale of 1V/div). Experimental results clearly show that the potential difference between the two dc link capacitors is kept below 1V.

The efficiency of the proposed NPC inverter fed PMSM drive with the TLBC has been calculated experimentally by varying the load from 0.5 Nm to 4.5 Nm, with an input dc supply of 200 V. The obtained efficiency has been verified with the conventional NPC inverter fed PMSM drive without the TLBC by selecting an input dc voltage of 300 V as shown in Fig. 25. The experimental tests confirms that the proposed NPC inverter fed PMSM drive possess better efficiency when compared to [41] with the conventional zero direct axis current control i.e. $I_d = 0$ control.

V. Conclusions

This paper proposes a voltage balancing technique using a TLBC for a three-level NPC inverter fed permanent magnet synchronous motor drive. The advantage of this balancing circuit when compared to other carrier based PWM technique or SVM techniques is its boosting feature, which is in demand these days for the solar electric vehicle applications. The proposed MLI fed PMSM drive reduces the voltage THD and torque pulsation. The performance is enhanced when compared to the conventional two-level VSI fed PMSM drive. Cost effective software based position estimation for the proposed PMSM drive is also implemented and experimentally investigated. A detailed simulation study is carried out for the proposed drive system. Experimental results validate the simulation result for the proposed drive. The proposed drive can be very useful for electric vehicle applications when compared with two-level VSI fed drives.

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